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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,422	08/30/2000	Jeffrey W. Honeycutt	M122-1332	9935

21567 7590 07/23/2003

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/651,422	Applicant(s) HONEYCUTT ET AL.
	Examiner Jennifer M. Kennedy	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 30 June 2003 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 9,10,13 and 32-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9,10,13 and 32-35 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 17 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Notice to Applicant

Applicants' Request for Continued Examination and the accompanying amendments mailed June 30, 2003 has been entered and made of record as paper number 19 and 20 respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 13, 32 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Cho et al. (U.S. Patent No. 5,707,901).

Cho et al. discloses the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (18) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (25,26) along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least two different layers having different chemical compositions from one another; a first (25) of the at least two layers comprising Al_pO_q, wherein p, q, x, y, and z are greater than 0 and less than 10, the second (26) of the at least two layers consisting essentially of silicon and nitrogen, the first of the at least two layers is between the second of the at least two layers and the

transistor gate sidewall , anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall, the anisotropically etching comprising etching both of the first and second of the at least two layers; and depositing a dopant barrier layer (34) over the spacer and forming a doped oxide layer (35) over the barrier layer.

The examiner notes that Cho et al. refers to the dopant barrier layer (34) simply as a dielectric layer. The dielectric of Cho et al. will inherently act as a dopant barrier layer since any layer in between a doped layer and an underlying layer will in some measure slow or prevent out diffusion of the dopants in the doped layer.

Cho et al. also discloses the method wherein the first of the at least two layers is Al_2O_3 (see column 2, line 14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho et al. (U.S. Patent No. 5,707,901) in view of Ngo et al. (U.S. Patent No. 6,420,752).

Cho et al. discloses the method substantially as claimed and rejected above, but does not disclose the method wherein the dopant barrier layer comprises silicon dioxide or whereon the doped oxide layer comprises BPSG.

Ngo et al. teaches the method of forming a dopant barrier layer comprising silicon dioxide (260) and wherein the doped oxide layer comprises BPSG (232, see column 7, lines 40-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dopant barrier layer of Cho et al. silicon oxide since silicon oxide is recognized as a material that prevents out diffusion of dopants that could cause degradation of the underlying device. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer of BPSG since BPSG has good reflow characteristics allowing for planarization.

Claims 9, 10, 13, 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. Patent No. 5,915,182) in view of Tsukamoto et al. (U.S. Patent No. 5,700,349) and Ngo et al. (U.S. Patent No. 6,420,752).

Wu discloses the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (8) comprising a sidewall which comprises electrically conductive material; forming an electrically insulative material (10, 12) along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least two different layers having different chemical compositions from one another; a first (10) of the at least two layers

comprising Al_pO_q, wherein p, q, x, y, and z are greater than 0 and less than 10, the second (12) of the at least two layers consisting essentially of silicon and nitrogen, anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall, the anisotropically etching comprising etching both of the first and second of the at least two layers; and wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall (see column 3, lines 20-40).

Wu further discloses the method further comprising implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant (see column 3, lines 43-54 and Figures 4-5.

Wu does not disclose the method wherein the first of the at least two layers is Al_pO_q. Tsukamoto et al. disclose the method wherein an a spacer made of insulative material can be formed of silicon nitride, silicon oxynitride or aluminum oxide (see column 4, lines 40-50 and column 9, lines 24-34) all with the same basic desired effects. Thus, Tsukamoto et al. teaches that silicon oxynitride and aluminum oxide are functional equivalents in forming insulative spacers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first spacer of Wu with aluminum oxide rather than silicon oxynitride since silicon oxynitride and aluminum oxide are recognized as functional equivalents in the art and would result in the same basic desired effects.

Neither, Wu or Tsukamoto et al. disclose the method wherein a dopant barrier layer formed of silicon dioxide is formed over the spacer and a doped oxide layer of BPSG is formed over the barrier layer.

Ngo et al. discloses the method wherein a dopant barrier layer (260) formed of silicon dioxide is formed over the spacer and a doped oxide layer (232) of BPSG is formed over the barrier layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer over the device of Wu in order to allow further interconnection of the device without shorting. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer prior to forming the doped oxide layer in the combined method of Wu Tsukamoto et al. and Ngo et al. to prevent degradation caused by out diffusion of the dopants of the doped oxide layer.

Claims 9, 10, 13, 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (U.S. Patent No. 6,107,149) in view of Tsukamoto et al. (U.S. Patent No. 5,700,349) Ngo et al. (U.S. Patent No. 6,420,752).

Wu et al. discloses the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (21) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (24, 25) along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least two different layers having different chemical compositions from one another; a first (24) of the at least two

layers comprising Al_pO_q, wherein p, q, x, y, and z are greater than 0 and less than 10, the second (25)of the at least two layers consisting essentially of silicon and nitrogen, anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall, the anisotropically etching comprising etching both of the first and second of the at least two layers; and wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall (see column 4, line 65 through column 5, line 40).

Wu et al. further discloses the method further comprising implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant (see column 5, lines 40-59).

Wu et al. do not disclose the method wherein the first of the at least two layers is Al_pO_q. Tsukamoto et al. disclose the method wherein an a spacer made of insulative material can be formed of silicon nitride, silicon oxynitride or aluminum oxide (see column 4, lines 40-50 and column 9, lines 24-34) all with the same basic desired effects. Thus, Tsukamoto et al. teaches that silicon nitride, silicon oxynitride and aluminum oxide are functional equivalents. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first spacer of Wu et al. with aluminum oxide rather than silicon nitride or silicon oxynitride since silicon nitride, silicon oxynitride and aluminum oxide are recognized as functional equivalents in the art and would result in the same basic desired effects.

Neither, Wu et al. or Tsukamoto et al. disclose the method wherein a dopant barrier layer formed of silicon dioxide is formed over the spacer and a doped oxide layer of BPSG is formed over the barrier layer.

Ngo et al. discloses the method wherein a dopant barrier layer (260) formed of silicon dioxide is formed over the spacer and a doped oxide layer (232) of BPSG is formed over the barrier layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer over the device of Wu et al. in order to allow further interconnection of the device without shorting. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer prior to forming the doped oxide layer in the combined method of Wu et al., Tsukamoto et al. and Ngo et al. to prevent degradation caused by out diffusion of the dopants of the doped oxide layer.

Claims 9, 10, 13, 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ju et al. (U.S. Patent No. 6,232,166) in view of Tsukamoto et al. (U.S. Patent No. 5,700,349) and Ngo et al. (U.S. Patent No. 6,420,752).

Ju et al. discloses the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (30) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (36, 39) along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least two different layers having different

chemical compositions from one another; a first (36) of the at least two layers comprising Al_pO_q, wherein p, q, x, y, and z are greater than 0 and less than 10, the second (39) of the at least two layers consisting essentially of silicon and nitrogen, anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall, the anisotropically etching comprising etching both of the first and second of the at least two layers; and wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall (see column 6, lines 7-59).

Ju et al. further discloses the method further comprising implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant (see column 6, line 60-Column 70, line 6).

Ju et al. discloses the method substantially as claimed, and rejected above, but do not disclose the method wherein the first of the at least two layers is Al_pO_q. Tsukamoto et al. disclose the method wherein an a spacer made of insulative material can be formed of silicon nitride, silicon oxynitride or aluminum oxide (see column 4, lines 40-50 and column 9, lines 24-34) all with the same basic desired effects. Thus, Tsukamoto et al. teaches that silicon nitride, silicon oxynitride and aluminum oxide are functional equivalents. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first spacer of Ju et al. with aluminum oxide rather than silicon nitride or silicon oxynitride since silicon nitride, silicon oxynitride and aluminum oxide are recognized as functional equivalents in the art and would result in the same basic desired effects.

Neither, Ju et al. or Tsukamoto et al. disclose the method wherein a dopant barrier layer formed of silicon dioxide is formed over the spacer and a doped oxide layer of BPSG is formed over the barrier layer.

Ngo et al. discloses the method wherein a dopant barrier layer (260) formed of silicon dioxide is formed over the spacer and a doped oxide layer (232) of BPSG is formed over the barrier layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer over the device of Ju et al. in order to allow further interconnection of the device without shorting. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer prior to forming the doped oxide layer in the combined method of Ju et al., Tsukamoto et al. and Ngo et al. to prevent degradation caused by out diffusion of the dopants of the doped oxide layer.

Claims 9, 10, 13, 32, 33, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. Patent No. 5,915,182) in view of Tsukamoto et al. (U.S. Patent No. 5,700,349).

Wu discloses the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (8) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (10, 12) along the electrically conductive material of the transistor gate sidewall, the

electrically insulative material comprising at least two different layers having different chemical compositions from one another; a first (10) of the at least two layers comprising Al_pO_q, wherein p, q, x, y, and z are greater than 0 and less than 10, the second (12) of the at least two layers consisting essentially of silicon and nitrogen, anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall, the anisotropically etching comprising etching both of the first and second of the at least two layers; and wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall (see column 3, lines 20-40).

Wu further discloses the method further comprising implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant (see column 3, lines 43-54 and Figures 4-5.

Wu does not disclose the method wherein the first of the at least two layers is Al_pO_q. Tsukamoto et al. disclose the method wherein an a spacer made of insulative material can be formed of silicon nitride, silicon oxynitride or aluminum oxide (see column 4, lines 40-50 and column 9, lines 24-34) all with the same basic desired effects. Thus, Tsukamoto et al. teaches that silicon oxynitride and aluminum oxide are functional equivalents in forming insulative spacers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first spacer of Wu with aluminum oxide rather than silicon oxynitride since silicon oxynitride and aluminum oxide are recognized as functional equivalents in the art and would result in the same basic desired effects.

Wu also does not disclose the method of forming a dopant barrier layer and a doped oxide of BPSG. Tsukamoto et al. disclose the method wherein a dopant barrier layer (9) is formed over the spacer and a doped oxide layer of BPSG (10) is formed over the barrier layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer over the device of Wu in order to allow further interconnection of the device without shorting. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer prior to forming the doped oxide layer in the combined method of Wu and Tsukamoto et al. to prevent degradation caused by out diffusion of the dopants of the doped oxide layer.

The examiner notes that Tsukamoto et al. refers to the dopant barrier layer (9) as a etch stop layer. The etch stop layer of Tsukamoto et al. will inherently act as a dopant barrier layer since any layer in between a doped layer and an underlying layer will in some measure slow or prevent out diffusion of the dopants in the doped layer.

Claims 9, 10, 13, 32, 33, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (U.S. Patent No. 6,107,149) in view of Tsukamoto et al. (U.S. Patent No. 5,700,349).

Wu et al. discloses the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (21) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (24, 25) along the electrically conductive material of the transistor gate

sidewall, the electrically insulative material comprising at least two different layers having different chemical compositions from one another; a first (24) of the at least two layers comprising Al_pO_q, wherein p, q, x, y, and z are greater than 0 and less than 10, the second (25)of the at least two layers consisting essentially of silicon and nitrogen, anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall, the anisotropically etching comprising etching both of the first and second of the at least two layers; and wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall (see column 4, line 65 through column 5, line 40).

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electrically insulative material comprising at least two different layers having different chemical compositions from one another; a first (36) of the at least two layers comprising Al_pO_q, wherein p, q, x, y, and z are greater than 0 and less than 10, the second (39) of the at least two layers consisting essentially of silicon and nitrogen, anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall, the anisotropically etching comprising etching both of the first and second of the at least two layers; and wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall (see column 6, lines 7-59).

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Ju et al. discloses the method substantially as claimed, and rejected above, but do not disclose the method wherein the first of the at least two layers is Al_pO_q. Tsukamoto et al. disclose the method wherein an a spacer made of insulative material can be formed of silicon nitride, silicon oxynitride or aluminum oxide (see column 4, lines 40-50 and column 9, lines 24-34) all with the same basic desired effects. Thus, Tsukamoto et al. teaches that silicon nitride, silicon oxynitride and aluminum oxide are functional equivalents. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first spacer of Ju et al. with aluminum oxide rather than silicon nitride or silicon oxynitride since silicon nitride, silicon oxynitride and

aluminum oxide are recognized as functional equivalents in the art and would result in the same basic desired effects.

Ju et al. also does not disclose the method of forming a dopant barrier layer and a doped oxide of BPSG. Tsukamoto et al. disclose the method wherein a dopant barrier layer (9) is formed over the spacer and a doped oxide layer of BPSG (10) is formed over the barrier layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer over the device of Wu in order to allow further interconnection of the device without shorting. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer prior to forming the doped oxide layer in the combined method of Ju et al. and Tsukamoto et al. to prevent degradation caused by out diffusion of the dopants of the doped oxide layer.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (703) 308-6171. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmk
July 16, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800